2A Ultra Low Dropout Linear Regulator

General Description

The uP0109 is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 2A output current.

This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output. The output voltage is tightly regulated to track reference voltage input within 20mV variation with fast to line/load transient.

Other features include chip shutdown function, soft-start, on-chip thermal protection, and bi-directional current limit protection. The uP0109 is available in PSOP-8L, FSOP-8L, WDFN3x3-8L packages with very low thermal resistance.

Applications

- **Desktop PCs, Notebooks, and Workstations**
- **Graphic Cards**
- **Low Voltage Logic Supplies**
- **Microprocessor and Chipset Supplies**
- **Split Plane Microprocessor Supplies**
- **Advanced Graphics Cards Supplies**
- **SoundCards and Auxiliary Power Supplies**
- **SMPS Post Regulators**

Features

- **Generate Termination Voltage for DDR Memory Interface**
  - **Output Voltage Traces Reference Input**
  - **Capable of Sinking/Sourcing 2A**
  - **Integrated Low $R_{DS(ON)}$ MOSFETs**
  - **Excellent Line and Load Regulation**
- **Low External Part Count**
- **Bidirectional Current Limit Protection**
- **On-Chip Thermal Protection**
- **Support Pure MLCC**
- **RoHS Compliant and Halogen Free**

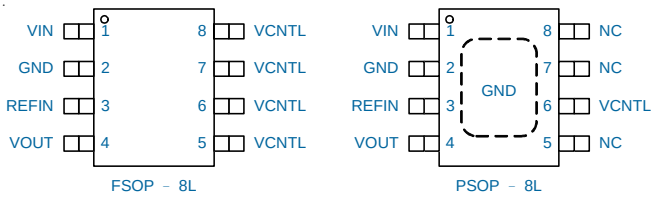
Ordering Information

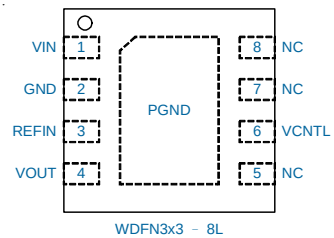
Order Number	Package Type	Top Marking
uP0109PSW8	PSOP-8L	uP0109P
uP0109PSF8	FSOP-8L	uP0109P
uP0109PDD8	WDFN3x3-8L	uP0109P

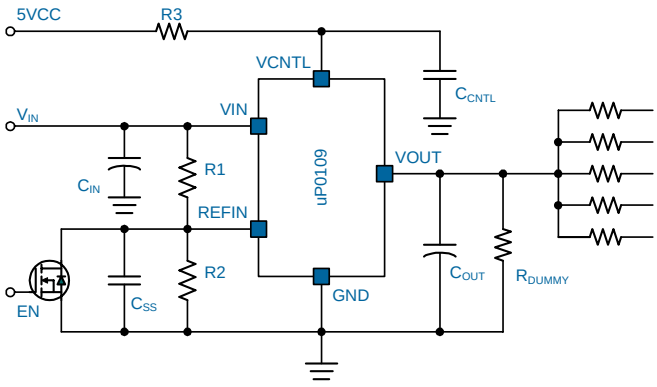
Status:
In Production: uP0109PSW8
Others: Please check the sample/production availability with uPI representatives.

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit



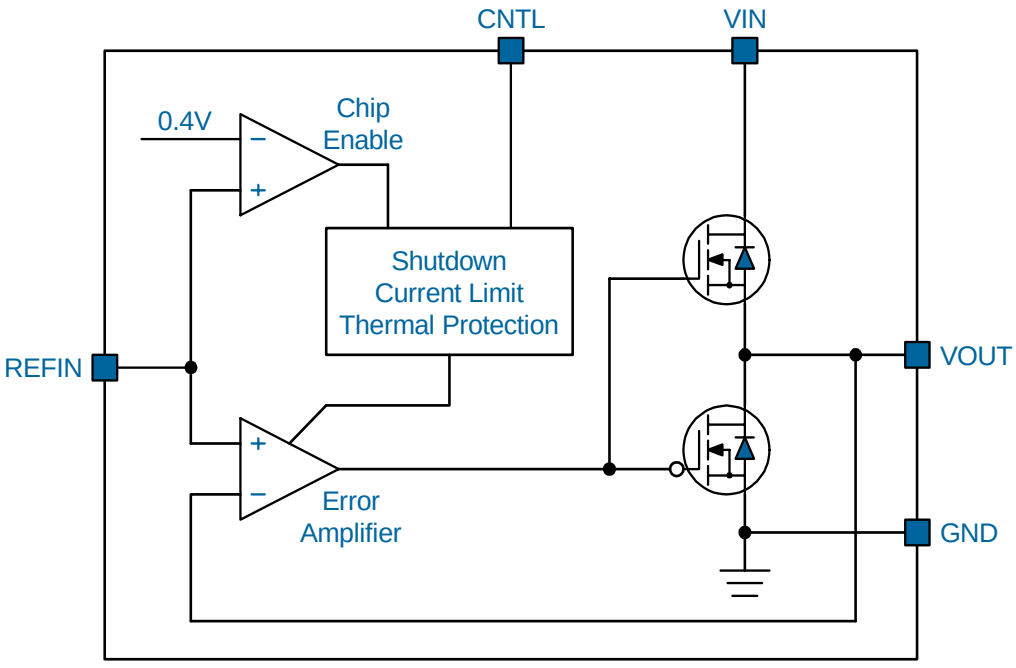




Functional Pin Description

Pin No.	Name	Pin Function
1	VIN	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Large bulk capacitors with low ESR should be placed physically close to this pin to prevent the input rail from dropping during large load transient. A 10uF ceramic capacitor is recommended at this pin. V_{IN} cannot be forced higher than V_{CNTL} otherwise the current limit function may be false triggered and disable the output voltage.
2	GND	**Ground.**
3	REFIN	**Reference Voltage Input.** This pin is the non-inverting input of the error amplifier. The output voltage is regulated to track the reference voltage input. This pin is also monitored by the shutdown comparator. Pulling this pin lower than 0.15V shuts down this device.
4	VOUT	**Output Voltage.** This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin. To maintain adequate transient response to large load change, typical value of 1000uF Al electrolytic capacitor with 10uF ceramic capacitors are recommended to reduce the effects of current transients on VOUT.
5, 7, 8	NC	**Not Internally Connected.**
6	VCNTL	**Supply Input for Control Circuit.** This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the V_{VCNTL}. For the device to regulate, the voltage on this pin must be at least 2.0V greater than the output voltage, and no less than $V_{CNTL\_MIN.}$ V_{CNTL} input voltage must be ready before V_{IN} input voltage.
Exposed Pad	GND	**Ground.** The exposed pad acts the dominant power dissipation path and should be soldered to well design PCB pads as described in the *Application Informations Chapter.*

Functional Block Diagram



Functional Description

Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal value. Dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under the conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under the conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load.

The quiescent current I_Q is defined as the supply current used by the regulator itself that does not pass into the load. It typically includes all bias currents required by the LDO and any drive current for the pass transistor.

General

The uP0109 is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 2A output current.

This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output. The output voltage is tightly regulated to track reference voltage input within 20mV variation with fast to line/load transient.

Other features include chip shutdown function, soft-start, on-chip thermal protection, and bi-directional current limit protection.

Power On Reset

The uP0109 mainly consists of power on reset and chip enable, pass transistors, current limit, error amplifier and temperature protection as shown in *Functional Block Diagram*. The uP0109 continuously monitors control input and power input for power on reset (POR) to ensure the device can work properly. The typical POR rising levels are 2.7V and 0.6V for control input and power input respectively.

Chip Enable and Soft Start

Once POR is granted, the uP0109 is ready for normal operation. The REFIN pin is a dual-function input pin: reference input and shutdown control input. A singal level transistor is adequate to pull this pin lower than 0.15V and shuts down the device reducing the shutdown current below 50uA.

The uP0109 tightly regulates the output voltage to track V_{REFIN} if it is higher than 0.4V. The output voltage ramp up/down speed is limited as 5.7mV/us to limit inrusht current form power input as shown in Figure 1. The inrush current to charge/discharge the output capacitor is calculated as:

$$I_{INRUSH} = 5.7mV/us \times C_{OUT}$$

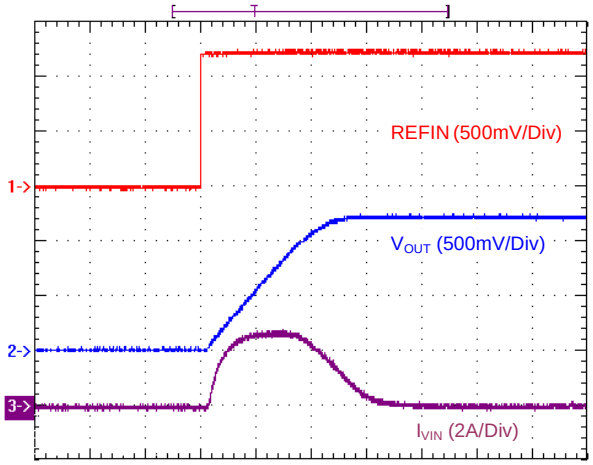


Figure 1. Chip Enable and Soft Start

A 100uF output capacitor will demand 0.5V input current during softstart. If the output capacitor is larger than 470uF, current limit function may be activated and limit the inrush current to about 2.2A. Make sure the power input is capable of delivering inrush current with selected output capacitor.

Output Voltage Regulation

The output voltage is tightly regulated to track the reference voltage applied at REFIN pin. The error signal is amplified to control the gates of NMOSFET for sourcing current from

VIN and singing current GND respectively. Since the gate voltage is provided by the control input V_{CNTL}, it is highly recommended the control input is 2V higher than the output voltage to achieve tight regulation and fast transient response.

Current Limit

The uP0109 monitors sourcing and sinking ouput currents. The output currents are limited to a safe level by reducing the gate voltages of the NMOSFET during output overload or short circuit. The output voltage is reduced if the load continuously demands current higher than the current limit level. The output voltage is re-built up when overload or short circuit conditions are removed.

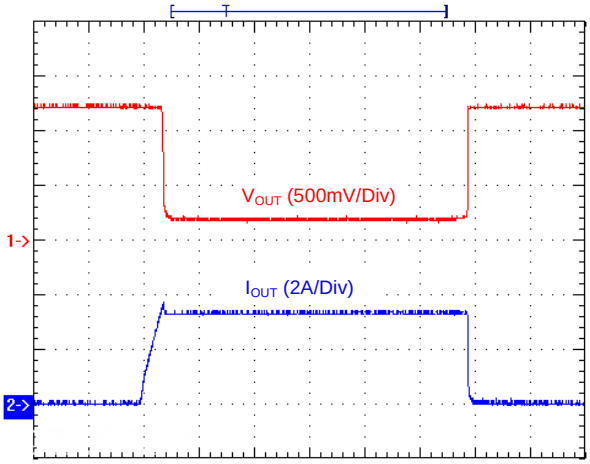


Figure 1. VOUT Output Source Current Limit

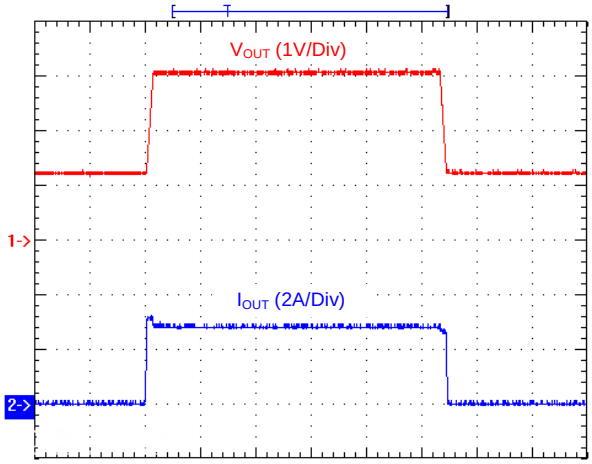


Figure 2. VOUT Output Sink Current Limit

Thermal Protection

The uP0109 implements a thermal shutdown function to protect the device from damage when output overload or short circuit. Both NMOSFETs are turned off when the juction temperature exceeds about 170°C, allowing the junction temperature to cool down. The output voltage is re-built up when the junction temperature reduces by 40°C, resulting in a pulsed output during continuous thermal over load conditions.

The thermal protection is designed to protect the device from damage during abnormal operation. It is highly recommended to keep the maximum junction temperature under 150°C during normal operation for maximum realiability.

Absolute Maximum Rating

(Note 1)

Control Input Voltage V_{CNTL} (Note 1) ---------- -0.3V to +7V
Power Input Voltage V_{IN} ---------- -0.3V to +7V
Other Pins ---------- -0.3V to (V_{CNTL} + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
PSOP-8L θ_{JA} ---------- 50°C/W
PSOP-8L θ_{JC} ---------- 5°C/W
FSOP-8L θ_{JA} ---------- 90°C/W
FSOP-8L θ_{JC} ---------- 35°C/W
WDFN3x3-8L θ_{JA} ---------- 60°C/W
WDFN3x3-8L θ_{JC} ---------- 5°C/W
Power Dissipation, P_D @ T_A = 25°C
PSOP-8L ---------- 2.0W
FSOP-8L ---------- 1.11W
WDFN3x3-8L ---------- 1.67W

Recommended Operation Conditions

(Note 2)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CNTL} ---------- +2.8V to +6.0V
Power Input Voltage, V_{IN} ---------- +1.0V to V_{CNTL}

Electrical Characteristics

(V_{CNTL} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
POR Threshold	$V_{CNTLRTH}$	V_{CNTL} Rising	--	2.7	2.8	V
POR Hysteresis	$V_{CNTLHYS}$	V_{CNTL} Falling	--	0.2	--	V
Control Input Current in Shutdown	I_{CNTL_SD}	V_{CNTL} = V_{IN} = 5.0V, I_{OUT} = 0A, V_{REFIN} = 0V	--	50	90	uA
Control Input Current	I_{CNTL}	V_{CNTL} = 5.0V, V_{IN} = 1.8V, V_{REFIN} = 0.9V, I_{OUT} = 0A.	--	0.5	1.5	mA
Output Voltage						
Output Voltage Offset	V_{OS}	V_{CNTL} = 5.0V, V_{IN} = 1.8V, V_{REFIN} = 0.9V, I_{OUT} = 0A.	-20	--	+20	mV
Load Regulation	ΔV_{LOAD}	-1A < I_{OUT} < 1A	-20	--	+20	mV
Dropout Voltage	$V_{DROPOUT}$	V_{CNTL} = 4.5V, I_{OUT} = 1.5A, VOUT = 1.25V	--	225	525	mV
		V_{CNTL} = 4.5V, I_{OUT} = 1.0A, VOUT = 1.25V	--	150	350	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
Current Limit	I_{LIMIT_SOURCE}	V_{IN} = 1.8V, V_{OUT} = 0.9V, Sourcing	2.3	--	--	A
	I_{LIMIT_SINK}	V_{IN} = 1.8V, V_{OUT} = 0.9V, Sinking	2	--	--	
Short Circuit	I_{SC_VIN}	VOUT short circuit to VIN, Sinking	1	--	--	A
	I_{SC_GND}	VOUT short circuit to GND, Sourcing	1.5	--	--	A
REFIN Enable/Shutdown						
REFIN Logic High Threshold	V_{ENH}	REFIN rising to enable the device	0.4	--	--	V
REFIN Logic Low Threshold	V_{ENL}	REFIN falling to disable the device	--	--	0.15	V
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		--	30	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

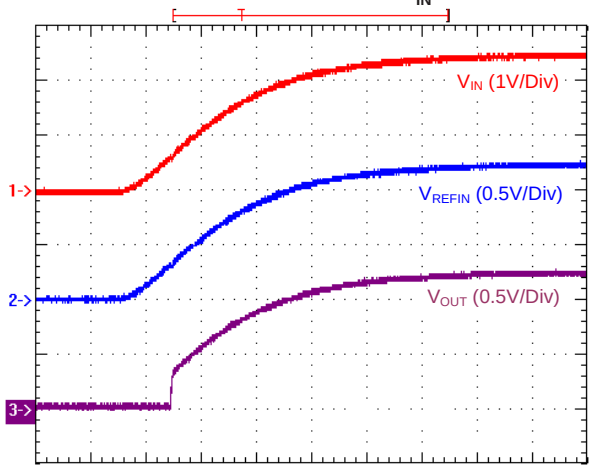
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

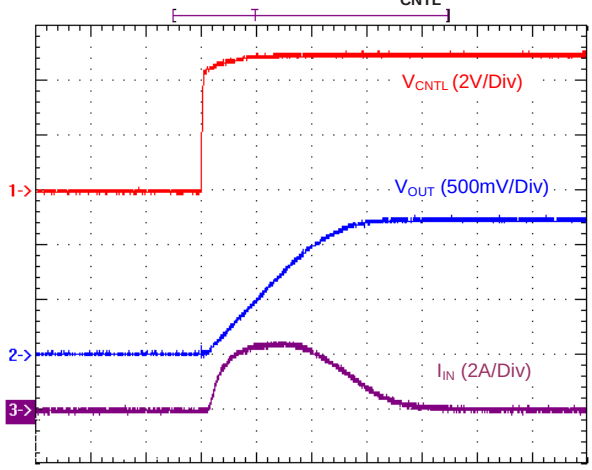
Typical Operation Characteristics

Power On From V_{IN}



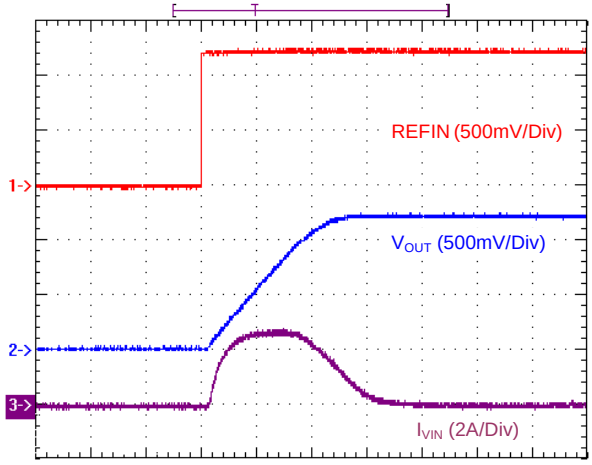
Time: 2ms/Div
V_{CNTL} = 5V, V_{REFIN} = 1.25V, C_{OUT} = 470uF

Power On from V_{CNTL}



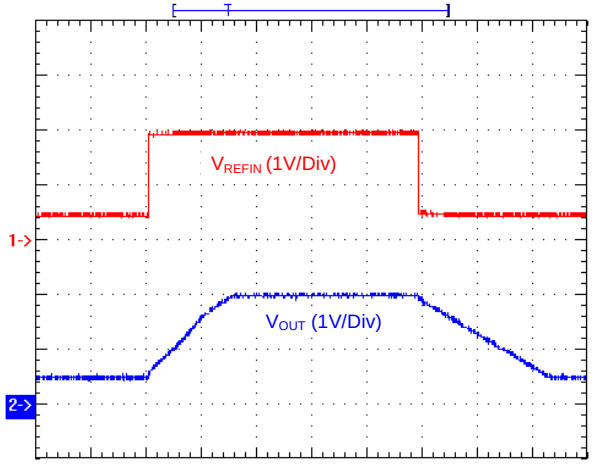
Time: 100us/Div
V_{IN} = 2.5V, V_{REFIN} = 1.25V, C_{OUT} = 470uF

Trun On from REFIN



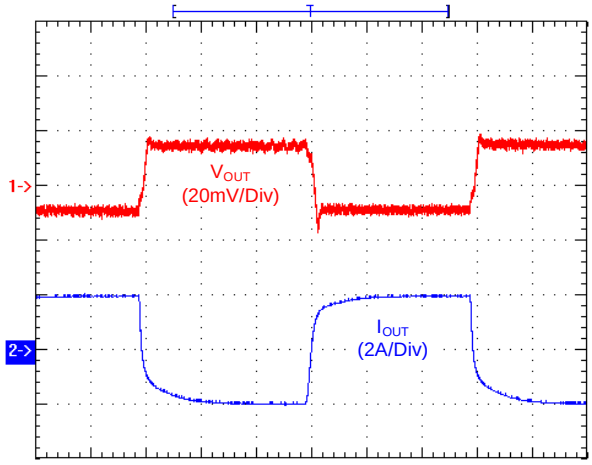
Time: 100us/Div
V_{IN} = 2.5V, V_{CNTL} = 5V, C_{OUT} = 470uF

REFIN Step Change



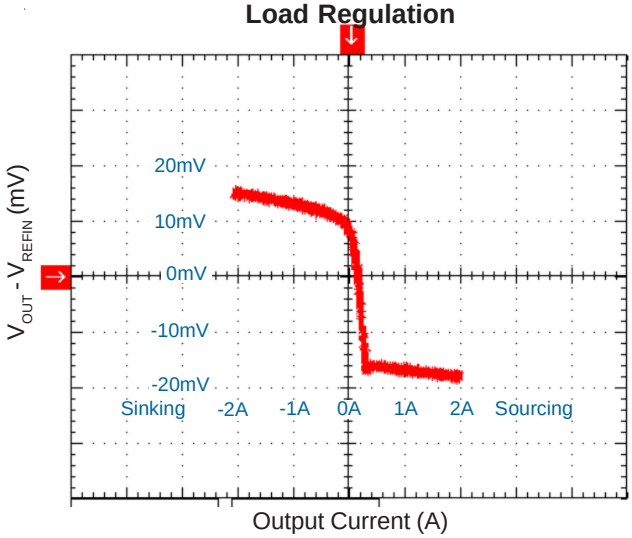
Time: 200us/Div
V_{IN} = 2.5V, V_{CNTL} = 5V, C_{OUT} = 1000uF

Load Transient Response



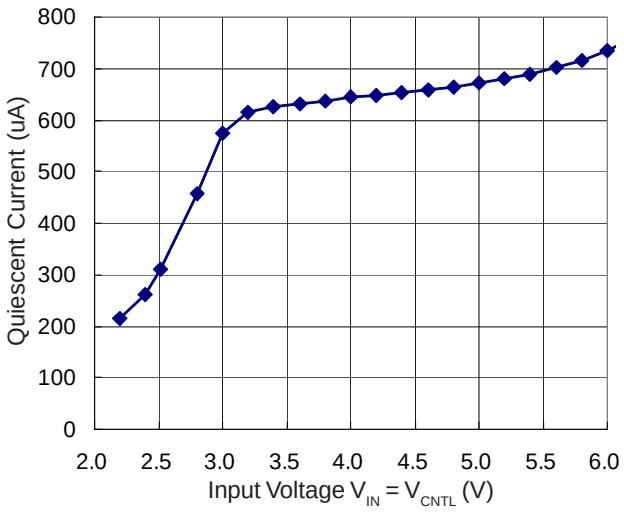
Time: 100us/Div
V_{IN} = 2.5V, V_{CNTL} = 5V, C_{OUT} = 1000uF

Load Regulation

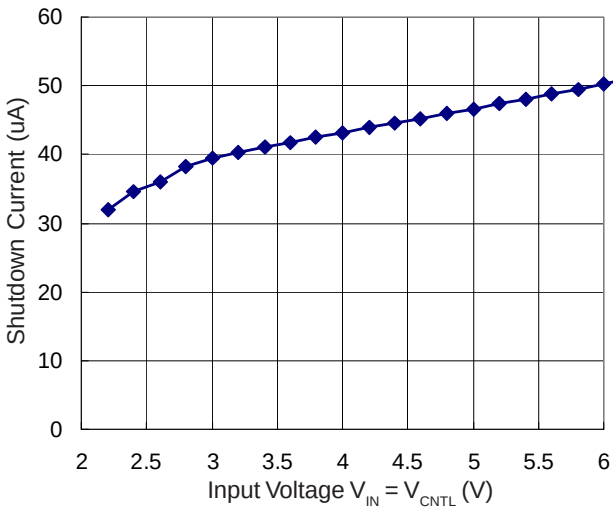


Typical Operation Characteristics

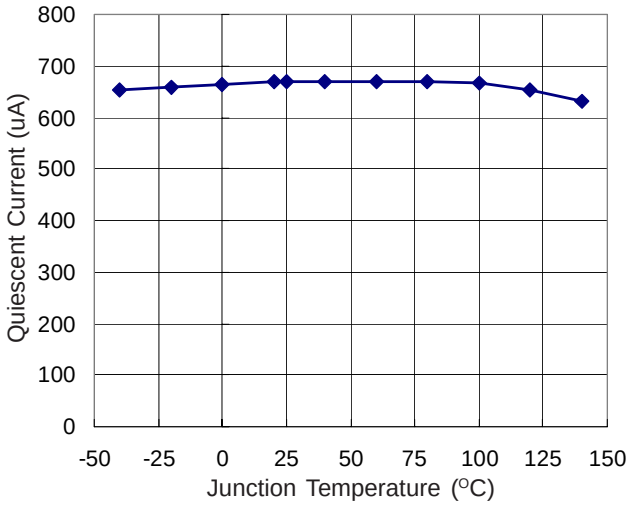
Quiescent Current vs. Input Voltage



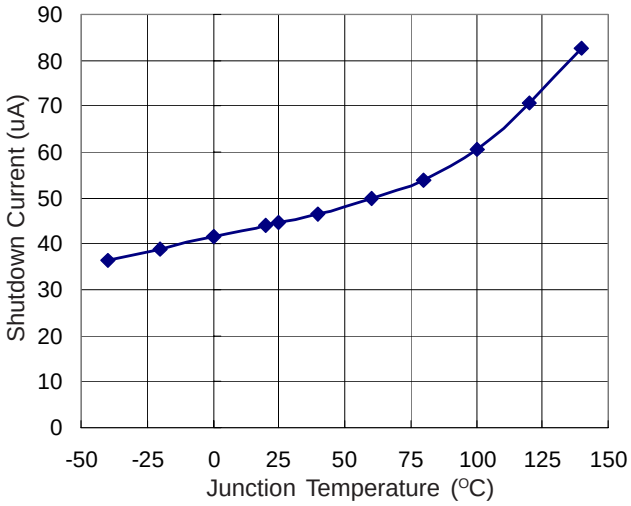
Shutdown Current vs. Input Voltage



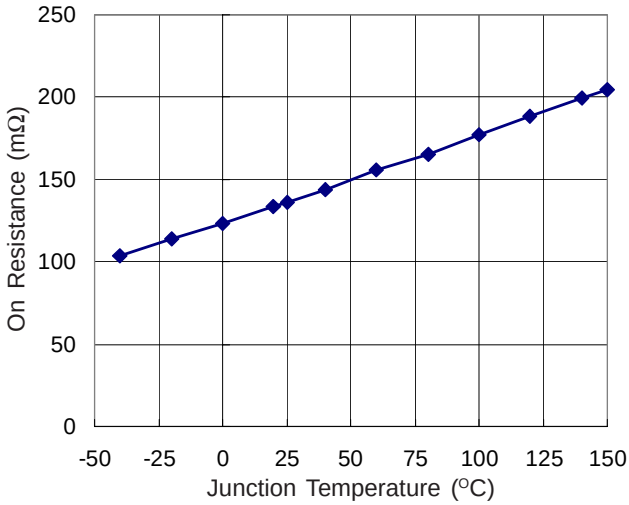
Quiescent Current vs. Temperature



Shutdown Current vs. Temperature



On Resistance vs. Temperature



VCNTL = 5.0V, For Both Sink and Source

Application Information

The uP0109 is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 2A output current. The output voltage is tightly regulated to track reference voltage input within 20mV variation with fast to line/load transient.

Supply Voltage for Control Circuit V_{CNTL}

This uP0109 works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output.

The control input provides bias current for control circuit and gate voltage for turning on and off the NMOSFETs. It is highly recommended to keep the control input 2.0V higher than the output voltage for optimal performance. Connect VCNTL pin to a 5V voltage source when available. The control voltage should be locally bypassed by a minimum 1uF ceramic capacitor plus a 10Ω resistor.

Power Input V_{IN} and Input Capacitor C_{CNTL}, C_{IN}

The VIN pin supplies current to output when the upper MOSFET turns on. The uP0109 is designed to work with minimum 10uF ceramic input capacitor. However, a bulk capacitor is still recommended in parallel with the ceramic capacitor to stabalize the input voltage during output soft start and load transient.

Since both power and control inputs are independently monitored for power on reset, special power sequence concern is not required for control input and power input.

When work with large output capacitor, the uP0109 may demand large input current during soft start. Make sure the power input is capable of delevering up to 3A.

Component	Recommended Value
C_{CNTL}/C_{IN}	Minimum 1uF/10uF Ceramic Capacitor

Note: A low-ESR 1uF/10uF capacitor with minimal susceptibility to temperature is recommended, and stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. The C_{IN} total capacitance of input capacitors value including ceramic and aluminum electrolytic capacitors should be larger than 10uF. A 1uF ceramic capacitor (C_{CNTL}) or higher is recommended for noise decoupling.

Reference Input

The output voltage is regulated to track the reference input at REFIN pin. The reference input can be obtained from power input by voltage divider or from an independent voltage reference. A ceramic capacitor physically near the IC is required to filter the refernce voltage.

Output Voltage and Output Capacitor, C_{OUT}

The uP0109 is designed to work with low ESR ceramic capacitors. No special concern is required on ESR for stable operation. A minimum bulk capacitance of 10uF, along with a 0.1uF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the uP0109 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Component	Recommended Value
C_{OUT}	Minimum 10uF Ceramic Capacitor

Note: A 10uF ceramic capacitor is recommended, and actual stability is highly dependent on temperature and load conditions. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) exacerbates output voltage fluctuation under rapid load change conditions. Total output capacitors value including ceramic and aluminum electrolytic capacitors should be larger than 10uF.

Thermal Consideration

The uP0109 integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°C for maximum reliability.

Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$$

It is adequate to neglect power loss with respective to control circuit $V_{CNTL} \times I_{CNTL}$ when considering thermal management in uP0109. Take the following moderate operation condition as an example: V_{IN} = 2.5V, V_{OUT} = 1.5V, I_{OUT} = 1A, the power dissipation is:

$$P_D = (2.5V - 1.5V) \times 1A = 1.0W$$

This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry

of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (θ_{JA}):

$\theta_{JA} = (T_J - T_A) / P_D$

θ_{JA} specified in the *Thermal Information* section is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for PSOP-8 package.

Given power dissipation P_D, ambient temperature and thermal resistance θ_{JA}, the junction temperature is calculated as:

$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. θ_{JA} of PSOP-8 packages is 75°C/W on JEDEC 51-7 (4 layers, 2S2P) thermal test board with minimum copper area. The maximum power dissipation at T_A = 25°C can be calculated as:

$P_{D(MAX)}$ = (125°C - 25°C) / 75°C/W = 1.33W

The thermal resistance θ_{JA} highly depends on the PCB design. Copper plane under the exposed pad is an effective heatsink and is useful for improving thermal conductivity. Figure 3 shows the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at T_A = 25°C. A 50mm² copper plane reduces θ_{JA} from 75°C/W to 50°C/W and increases maximum power dissipation from 1.33W to 2W.

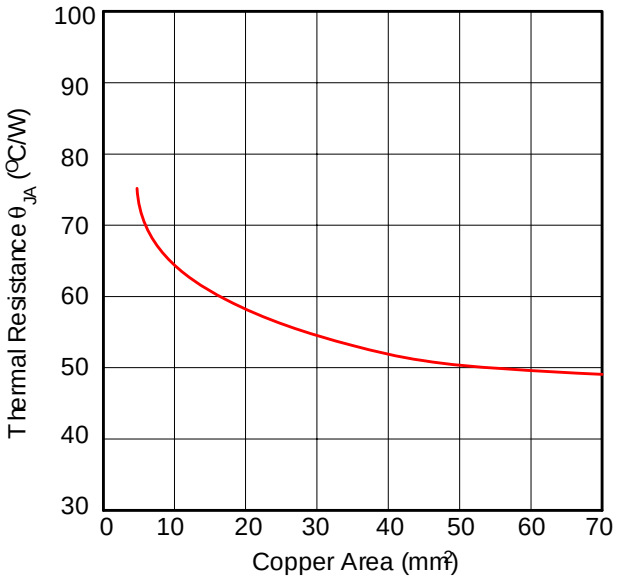


Figure 3. Thermal Resistance θ_{JA} vs. Copper Area

Figure 4 illustrated the recommended PCB layout for best thermal performance.

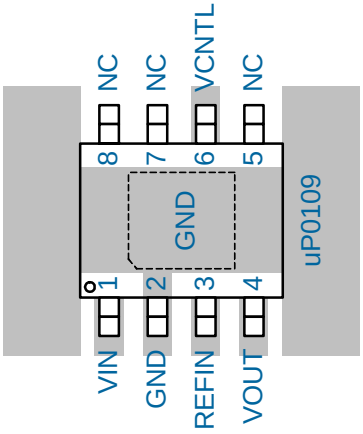


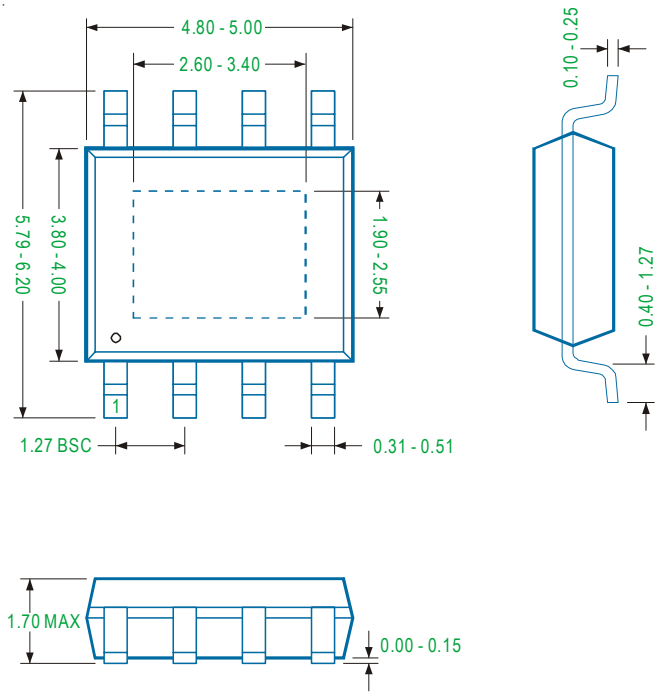
Figure 4. Recommended PCB Layout.

Layout Consideration

1. Place a local bypass capacitor as closed as possible to the VIN pin. Use short and wide traces to minimize parasitic resistance and inductance.
2. The exposed pad should be soldered on GND plane with maximum area and with multiple vias to inner layer of ground place for improved thermal performance.
3. Connect voltage divider directly to the point where regulation is required. Place voltage divider close to the device.

Package Information

PSOP-8 Package

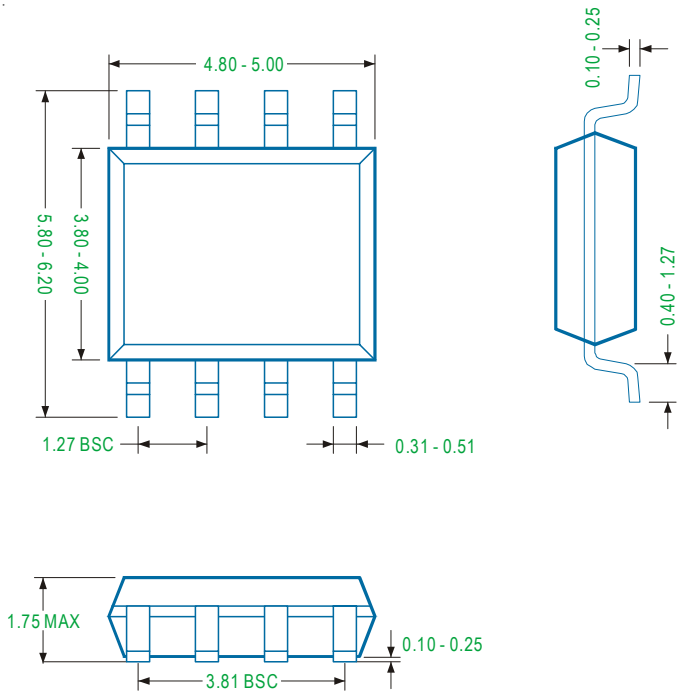


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

FSOP-8 Package



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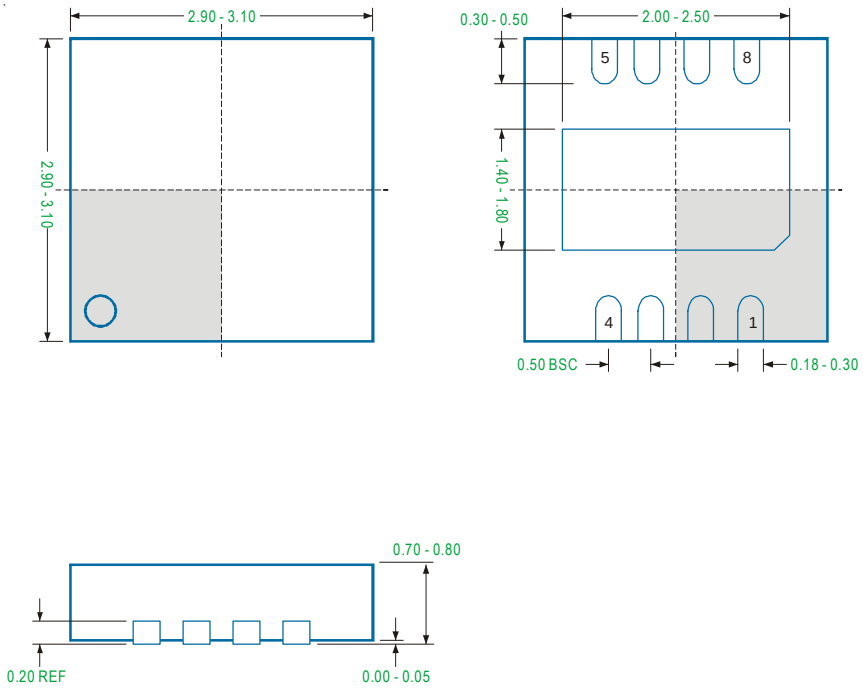
Package Information

WDFN3x3-8L



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